REMARKS

In the Office Action, claims 1-4 and 6-9 were rejected under 35 USC §102(e) as being anticipated by Tanaka. Claims 5 and 10 were rejected under 35 USC §103(a) as being unpatentable over Tanaka in view of Pinter.

The Examiner regards the present invention as being anticipated by U.S. Patent No. 6,600,225 to Tanaka. The Examiner attempts to read the features of the present invention onto Tanaka, wherein it is nowhere mentioned that the layered electronic device is a thin film memory device, but the Examiner's rendering "particularly a thin-film device for storing or processing of data" appears without foundation. Fig. 1 in Tanaka of course only discloses a section of conductive members formed between conductive lines in a semiconductor device. The conductive members are formed as respective rectangular bars 2 and 4, the former having a width equal to a line width of a first conductive line and the second having a width equal to the width of a second conductive line. The electrical connections established by two conductive memories being formed in the space between said conductive lines. This all together implies a completely different geometry from that of the present invention, particularly as the conductive members are located in two different steps in adjoining, but differently oriented through-holes. This cannot of course be

equated with the present invention and moreover cannot by no means be considered anticipatory to the present invention.

The Examiner now proceeds to an argument against the claims of the present invention by referring to Fig. 9C of Tanaka, while keeping the argument entirely out of context. Figs. 9A, 9B and 9C all disclose steps of a fourth fabrication method. As stated by Tanaka it employs "a dual damascene process" (col. 11, lines 66 and 67). Figs. 9A-9C can of course be compared with Fig. 1A, showing two intersecting conductive elements 1 and 5 oriented perpendicularly to each other.

All Figs. 9A-9C as seen in direction x-x' in Fig. 1A, correspond to a cross section taken along the y-y' axis of Fig. 1A. Quite evidently the process as depicted therein is a two-stage process.

In col. 12, from the second section of Tanaka, it is first stated with reference to Fig. 9A that the dielectric film forming a first interlayer 3a is deposited on the surface of the dielectric film which forms a substrate for the lower conductive layer. A trench 8 is formed in the dielectric film 3a. Films of a barrier material (e.g. titanium) and copper are deposited on the surface to form a metal layer filling the trench 8 and hence a lower conductive line 1 is formed by the metal filling this trench. As evident from Fig. 9A when compared with Fig. 1A, the lower layer conductor 1 is of course

shown in cross section and the overlying conductive member 2 can be thought of as an elongated metal piece deposited thereupon. A second interlayer dielectric film 3b is deposited over the entire surface and a rectangular hole 6 is formed in this second interlayer and aligned with part of the lower layer conductive line 1. Now yet another dielectric interlayer dielectric film 3c is also deposited as shown in Fig. 9B and by a dual photolithographic and etching process a trench 9 and rectangular hole 7 are formed in this dielectric film 3c. As stated the rectangular hole 7 is aligned below trench 9 and extends for part of the trench 9 and exposes part of the surface of the rectangular metal piece or bar 2, which was formed in a preceding step as a first conductive member.

With reference to Fig. 9C it is stated that films of the barrier metal and copper are deposited over the entire surface to form a metal layer that fills the rectangular hole 7 and the trench 9, and a rectangular metal bar 4 and an upper-layer conductive line 5 are formed simultaneously. This completes the formation of a wiring structure according to the first embodiment of the invention. However, this somewhat complicated procedure entails the formation of top and bottom conductive lines as well as a separate conductive member in the second step (Fig. 9B) and a very slight similarity with the present invention can only then be construed from the fact that

the upper conductive line 5 and the rectangular conductive member 4 are formed in one and the same process step. The resulting structure in Fig. 9C may for instance be compared with Fig. 1 C with the corresponding parts having the same reference numerals. The difference here between Fig. 1C and Fig. 9C is a transposition in the latter of the conductive members 2 and 4 relative to each other and along the y axis.

The arguments in favor of this fourth fabrication method of Tanaka is that smaller device geometry use can be achieved with the advantage that forming the metal bar 4 and the upper-layer conductive line 5 in what Tanaka terms as a dual damascene process. As far as can be understood damascene here is taken to mean forming a metal bar from two different metals and in contrast with the present invention only one part of the via connection is formed in one and the same operation, namely in the dual damascene process for forming the metal bar 4 and applying the conductive line as a single metal layer and with only one metal deposition process. But overall and ignored by the Examiner three separate metal deposition processes are used in order to form the via connection and no less than three dielectric films are used in the fabrication process. All this is clearly set forth in Tanaka, col. 12, line 7 to col. 13 and including line 5.

Now it is also clearly seen that the Examiner's rendering of Tanaka et al., saying that the method is characterized by forming a plug and wire in one and the same step as used for applying the conductive material for a conducting part of an overlying circuit layer is incorrect as it is taken completely out of context, leaving out the previous steps where actually two metallizations are involved in addition to lying down three different dielectric layers. Also, only one part of the conducting member is provided integral with the overlying conducting path, while another part of the interlayer connection must be formed in a separate step. However, the status of claim 2 becomes irrelevant when one considers that the improvement of the independent claim 1 is not anticipated by Tanaka and that dependent claims shall be allowable in conjunction with an allowable independent claim. This also applies to the recitation of dependent claims 2, 3 and 4 in the present application, but none of these claims can be read onto Tanaka, for actually the via connection therein is formed by two conductive members which each and separately of course lies within the footprint or the exterior of each of respectively the overlying or underlying conductors, but the requirement set forth in dependent claims 2-4 of the present application of course applies to the via connection or the interlayer connection viewed as a whole.

In other words the Examiner's argumentation against the present invention on the basis of Tanaka is based on either reading the disclosure Tanaka out of context or by willfully applying a distorted version of the teachings of Tanaka in order to convey an impression of its anticipatory nature in regard of the present application. This is an unacceptable examination of a patent application.

In regard of the assertion that claims 5 and 10 are unpatentable over Tanaka in view of U.S. Patent No. 5,322,816 to Pinter, Pinter discloses electrical via connections in interconnect layers in integrated circuits and particularly are concerned with making via holes to such interconnect layers, the interconnect layer is used to separate two active circuit layers of multichip module as shown in Fig. 2. Pinter is not concerned with forming via connection between electrode structures in thin films but rather with forming circular via openings circular as indicated by the phrase "diameter of the aperture 20" in col. 3, line 40, and the text here continues to state that this diameter is approximately twice the thickness of the silicon film layer. In the same column, lines 8-10 this layer is stated to have a thickness in the range of approx. 10 micrometers to approx. 50 micrometers. Hence the technology as disclosed in Pinter is not at all directed to thin film technology and the interconnections of electrode structures

with width in the range down to the line widths obtainable with present design rules, i.e. in the range appreciably less than 1 micrometer and then preferably below 0.2 micrometers. What is clear from the description in Pinter in regard of the Figs. 1b -1d (col. 4, lines 3-61) is that Pinter is concerned with an entirely different process regardless of the dimensional features. This includes isolating the sloping walls of the etched via hole, a necessary requirement since the interconnect layers comprises a fairly thick silicon film 14 and then a separate contact element 26 is deposited in the via opening and extending down to a layer of bonding oxide 12 in the interconnect layer. It is stated that contact element 2c is formed by a blanket deposited metallization. Still, after this metallization no throughgoing via connection is formed and this requires additional steps from the underside of the interconnect layer, whereafter finally a backside contact 28 can be formed from depositing and patterning a suitable metal.

It can be safely concluded that neither Tanaka nor Pinter disclose the single-step process for forming a via connection as taught by the present invention. Both relies on at least two or more steps and the via metal in itself is formed by at least two contact pieces in two different processes. Of course, the tapered side walls of the via hole which in the present case only applies to the transversal

surface thereof and conformal with the electrode geometry. This in itself is different from the circular taper of the via hole of Pinter, although we can acknowledge that this feature may be selected in order to ease metallization and improve contact. But it should be noted that in the present case it also serves to strengthen the contact metal in itself by avoiding any sharp bends in the planar metallization. Again it should, however, be noted that the tapered end sides of the plug and wire according to the present invention only is the subject of a dependent claim and hence should be allowable in connection with an allowable independent claim.

The present invention is thus addressed to the solution of a completely different problem than is the case of the cited prior art, and as seen from the last section of the description the present invention is eminently suited for matrix-addressable devices due to the fact that such devices comprise a huge number of stripe electrodes that shall be connected downwards through an interlayer. So in a narrow sense the present invention is concerned with a suitable process for forming via contacts for so-called staggered via connections, which in case of the aforementioned devices provides for a much more cost-efficient and less real estate-consuming solution than for instance resorting to fan-out vias as shown in Fig. 1

of the present application and commonly used in the prior art, as one of ordinary skill in the art certainly will be aware of.

Based on the foregoing amendments and remarks, it is respectfully submitted that the claims in the present application, as they now stand, patentably distinguish over the references cited and applied by the Examiner and are, therefore, in condition for allowance. A Notice of Allowance is in order, and such favorable action and reconsideration are respectfully requested.

However, if after reviewing the above amendments and remarks, the Examiner has any questions or comments, he is cordially invited to contact the undersigned attorneys.

Respectfully submitted,

JACOBSON HOLMAN, PLLC

By: _____
Jonathan L. Scherer
Reg. No. 29,851

400 Seventh Street, N.W.
Washington, D.C. 20004-2201
(202) 638-6666

Date: February 23, 2005
JLS/dmt